

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 15

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte IAIN C. ROBERTSON, JEFFREY L. NYE, MICHAEL D. ASAL,
GRAHAM B. SHORT, RICHARD D. SIMPSON, and JAMES G. LITTLETON

Appeal No. 1998-0072
Application No. 08/476,786

ON BRIEF

Before URYNOWICZ, JERRY SMITH, and FRAHM, Administrative
Patent Judges.

JERRY SMITH, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on the appeal under 35 U.S.C. § 134
from the examiner's final rejection of claims 60, 62-64 and

Appeal No. 1998-0072
Application No. 08/476,786

66-73, which constituted all the pending claims in the application. An amendment after final rejection was filed on January 7, 1997 and was entered by the examiner. This amendment amended claims 60 and 66 and cancelled claims 62-64, 67, 72 and 73. In response to this amendment, the examiner indicated that claims 68-71 were now directed to patentable subject matter. Therefore, only claims 60 and 66 remain on appeal.

The disclosed invention pertains to a multifunction access circuit for use with first and second digital computers which can communicate with each other. More specifically, the invention consists of a dual-ported register file having first and second address decoders associated therewith. At least one of the address decoders is programmable to position it in an address space of a corresponding one of the computers.

Representative claim 60 is reproduced as follows:

60. A multifunction access circuit for use with first and second digital computers each having an address bus for supplying addresses and a data bus for transferring data, the access circuit comprising:

a register file having a first data port including inputs and outputs connected to the data bus of the first digital computer and a second data port including inputs and outputs connected to the data bus of the second digital computer, said register file having a plurality of storage locations for

Appeal No. 1998-0072
Application No. 08/476,786

storing data, and said register file capable of transferring data between said first data port and a first selected storage location simultaneously with transferring data between said second data port and a second selected storage location different from said first selected storage location;

a first address decoder connected to the address bus of the first computer and said register file, said first address decoder translating an address received on the address bus of the first computer into a first storage location of said register file;

a second address decoder connected to the address bus of the second computer and said register file, said second address decoder translating an address received on the address bus of the second computer into a second storage location of said register file; and

at least one of said first and second address decoders being programmable to position it in an address space of said corresponding first or second computer.

The examiner relies on the following references:

Bowers et al. (Bowers)	4,541,076	Sep. 10, 1985
Mason	4,694,426	Sep. 15, 1987
Ishikawa (Japanese Kokai)	2-123590	May 11, 1990

Claims 60 and 66 stand rejected under 35 U.S.C. § 103. As evidence of obviousness the examiner offers Mason in view of Ishikawa or Bowers.

Rather than repeat the arguments of appellants or the examiner, we make reference to the briefs and the answer for the respective details thereof.

OPINION

We have carefully considered the subject matter on appeal, the rejection advanced by the examiner and the evidence of obviousness relied upon by the examiner as support for the rejection. We have, likewise, reviewed and taken into consideration, in reaching our decision, the appellants' arguments set forth in the briefs along with the examiner's rationale in support of the rejection and arguments in rebuttal set forth in the examiner's answer.

It is our view, after consideration of the record before us, that the evidence relied upon and the level of skill in the particular art would not have suggested to one of ordinary skill in the art the obviousness of the invention as set forth in claims 60 and 66. Accordingly, we reverse.

Appellants have indicated that for purposes of this appeal claims 60 and 66 will stand or fall together as a single group [brief, page 3]. Consistent with this indication appellants have made no separate arguments with respect to these claims. Accordingly, both appealed claims before us will stand or fall together. Note In re King, 801 F.2d 1324,

Appeal No. 1998-0072
Application No. 08/476,786

1325, 231 USPQ 136, 137 (Fed. Cir. 1986); In re Sernaker, 702 F.2d 989, 991, 217 USPQ 1, 3 (Fed. Cir. 1983).

In rejecting claims under 35 U.S.C. § 103, it is incumbent upon the examiner to establish a factual basis to support the legal conclusion of obviousness. See In re Fine, 837 F.2d 1071, 1073, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). In so doing, the examiner is expected to make the factual determinations set forth in Graham v. John Deere Co., 383 U.S. 1, 17, 148 USPQ 459, 467 (1966), and to provide a reason why one having ordinary skill in the pertinent art would have been led to modify the prior art or to combine prior art references to arrive at the claimed invention. Such reason must stem from some teaching, suggestion or implication in the prior art as a whole or knowledge generally available to one having ordinary skill in the art. Uniroyal, Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 1051, 5 USPQ2d 1434, 1438 (Fed. Cir.), cert. denied, 488 U.S. 825 (1988); Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 293, 227 USPQ 657, 664 (Fed. Cir. 1985), cert. denied, 475 U.S. 1017 (1986); ACS Hosp. Sys., Inc. v. Montefiore Hosp., 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984). These showings by the

Appeal No. 1998-0072
Application No. 08/476,786

examiner are an essential part of complying with the burden of presenting a prima facie case of obviousness. Note In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992). If that burden is met, the burden then shifts to the applicant to overcome the prima facie case with argument and/or evidence. Obviousness is then determined on the basis of the evidence as a whole and the relative persuasiveness of the arguments. See Id.; In re Hedges, 783 F.2d 1038, 1039, 228 USPQ 685, 686 (Fed. Cir. 1986); In re Piasecki, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984); and In re Rinehart, 531 F.2d 1048, 1052, 189 USPQ 143, 147 (CCPA 1976). Only those arguments actually made by appellants have been considered in this decision. Arguments which appellants could have made but chose not to make in the brief have not been considered [see 37 CFR § 1.192(a)].

Mason teaches a system in which two computers can communicate with each other using a dual-ported RAM and a dual decoder. The examiner asserts that Mason does not teach an address bus coupling the decoders to the computers. The

examiner cites Ishikawa and Bowers as each teaching a dual port memory having dual address decoders responsive to address, data and control signals from distinct sources. It is the examiner's position that each of Ishikawa and Bowers teaches address decoders which are programmable to position a decoder in an address space of the corresponding computer. The examiner concludes that it would have been obvious to the artisan to use the dual decoder addressing schemes of Ishikawa or Bowers with the register file device of Mason [answer, pages 4-5].

Appellants argue that neither of the cited references teaches the claimed feature that "'at least one of said first and second address decoders is programmable to position it in an address space' of the corresponding computer" [brief, page 4]. With respect to Bowers and Ishikawa, appellants argue that neither reference teaches a programmable decoder and certainly not a decoder programmable to achieve the function recited in the claims [brief, pages 5-6; reply brief, page 2]. We agree with the position argued by appellants.

With respect to Ishikawa, we agree with appellants that the decoders 220 and 320 are not programmable. There is

nothing in the translation of the Ishikawa document that would suggest that either of these decoders is programmable.

Although the examiner states that "[a]ddress decoders 220 and 320 are designed to accept address inputs that place the memory in an address space of the accessing device (CPU)" [answer, page 4], there is nothing in Ishikawa to support this assertion of the examiner. Therefore, the rejection of the claims based on Mason and Ishikawa is not sustained.

With respect to Bowers, the examiner points to a logic gate array for teaching the programmability feature of the decoder as recited in the claims. The examiner states that "the gate array discussed throughout Bowers is specifically designed for creating customized logic functions within the decoders shown in figure 6" [answer, page 5]. According to the examiner, decoders formed from gate array logic cells meet the claim limitation quoted above.

We agree with appellants that the decoders in Bowers are neither programmable nor programmable "to position it in an address space of said corresponding first or second computer." With respect to the quoted function, the examiner never addresses this limitation specifically. The examiner

Appeal No. 1998-0072
Application No. 08/476,786

seems to be of the position that any decoder which is programmable would satisfy the language of the claims. We do not agree. A programmable decoder is not necessarily programmable to achieve the function recited in the claims.

We also agree with appellants that the logic gate array described in Bowers is not related to the decoders of the dual-ported memory. The logic gate array of Bowers merely provides programmability of how the data in the memory is to be used. The decoders shown in Figure 6 of Bowers are fixed decoders, that is not programmable, for the reasons argued by appellants. Since the decoders of Bowers are neither programmable nor programmable for the purpose recited in the claims, we do not sustain the rejection of the claims based on Mason and Bowers.

Appeal No. 1998-0072
Application No. 08/476,786

In summary, we have not sustained either of the examiner's alternative rejections of claims 60 and 66. Therefore, the decision of the examiner rejecting claims 60 and 66 is reversed.

REVERSED

STANLEY M. URYNOWICZ, JR.)	
Administrative Patent Judge)	
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JERRY SMITH)	BOARD OF PATENT
Administrative Patent Judge)	APPEALS AND
)	INTERFERENCES
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ERIC FRAHM)	
Administrative Patent Judge)	

Appeal No. 1998-0072
Application No. 08/476,786

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